CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7161
Digital Radio Processor

D/7161_FI-1.0/4 September 2013 **DATASHEET** Advance Information

7161FI-1 TDMA Digital Radio Processor

Features

Tx Functions:

- Two-point modulation analogue outputs
- Root-raised-cosine (α=0.2) pulse shaping
- RAMDAC capability for PA ramping control
- Tx trigger feature allowing precise control of burst start time
- Tx burst sequence for automatic RAMDAC ramping and hardware switching

Rx Functions:

- I/Q analogue inputs
- Rx channel filtering and root-raised-cosine (α=0.2) pulse shaping
- Data returned as hard-decision bits or 4-bit soft-decision LLR metrics
- Automatic frame sync detection
- Automatic tracking of symbol timing and input I/Q DC offsets

Slot timing functions:

- 30ms slot format (264-bit bursts)
- Internal slot clock and timing maintenance
- Automatic synchronisation to received channel
- Automatic sequencing of hardware control

Auxiliary Functions:

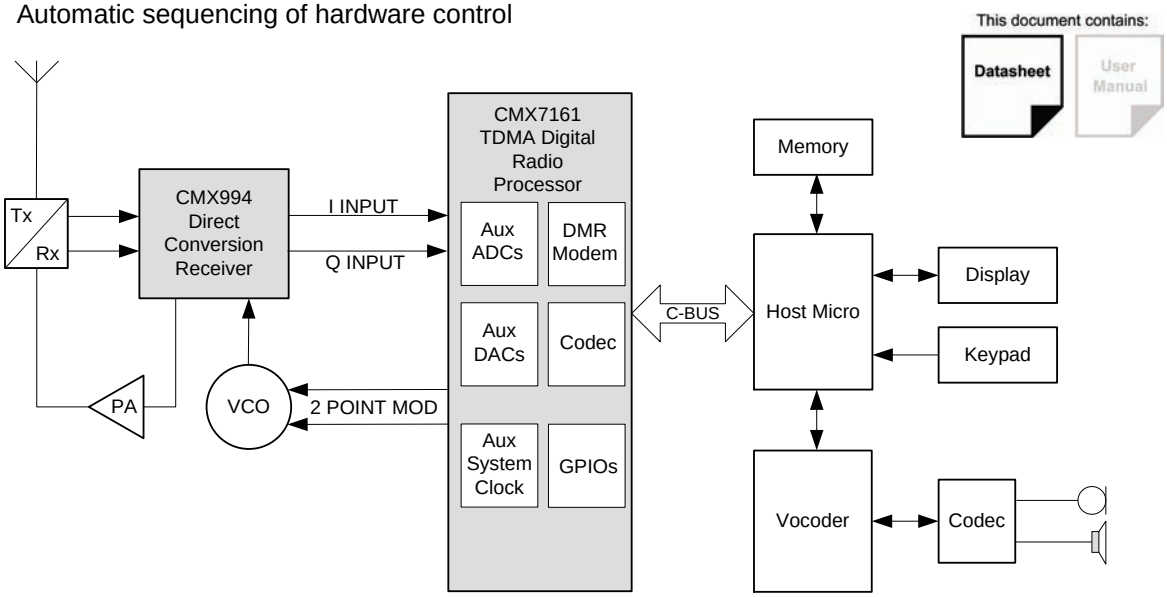
- Two programmable system clock outputs
- Four auxiliary ADCs with six selectable input paths
- SPI Thru-Port for interfacing to synthesisers and other serially controllable devices
- Four auxiliary DACs, one with built-in programmable RAMDAC

Host Interface:

- Optimised C-BUS (4-wire, high speed synchronous serial command/data bus) interface to host for control and data transfer, including streaming C-BUS for efficient data transfer
- Open drain IRQ to host
- Four GPIO pins
- Serial memory or C-BUS (host) boot mode.

Applications

- ETSI TS 102 361 Digital Mobile Radio (DMR)
- Police Digital Trunking (PDT) Radio



1 Brief Description

The CMX7161 FI-1.x is a half-duplex digital radio modem intended for use in two-slot TDMA systems such as the ETSI TS 102 361 standard for Digital Mobile Radio (DMR). It uses root-raised-cosine (α=0.2) 4-FSK modulation in a 12.5kHz channel. Slot timing and synchronisation are handled automatically by the device.

An integrated analogue interface supports direct connection to a device such as CML's CMX994 Direct Conversion Receiver and two-point modulation transmitter with few external components; no external codecs for the I/Q interface are required.

Intelligent auxiliary ADC, DAC and GPIO sub-systems are provided to minimise required host interaction and host I/O resources. Two synthesised system clock generators develop clock signals for off-chip use. The C-BUS/SPI master interface expands host C-BUS/SPI ports to control external devices.

The CMX7161 operates from a 3.3V supply and is available in 64-pin VQFN and LQFP packages.

The device uses CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™ data file which is uploaded during device initialisation to define the device's function and feature set. The Function Image™ can be loaded automatically from a host µC over the C-BUS serial interface or from an external memory device. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

This Data Sheet is the first part of a two-part document. Text shown in pale grey indicates features that will be supported in future versions.

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Figure Page

Information in this datasheet should not be relied upon for final product design. It is always recommended that you check for the latest product datasheet version on the CML website: [www.cmlmicro.com].

History

Version	Changes	Date (D/M/Y)
4	• Correction to deviation index bit symbol mapping table, Section 7.6	20/09/13
3	• Minor correction to Figure 7 – Outline Radio Design	02/09/13
2	• Updated document prepared for first alpha FI release	07/08/13
1	• Original document prepared for first alpha FI release	01/05/13

2 Block Diagrams

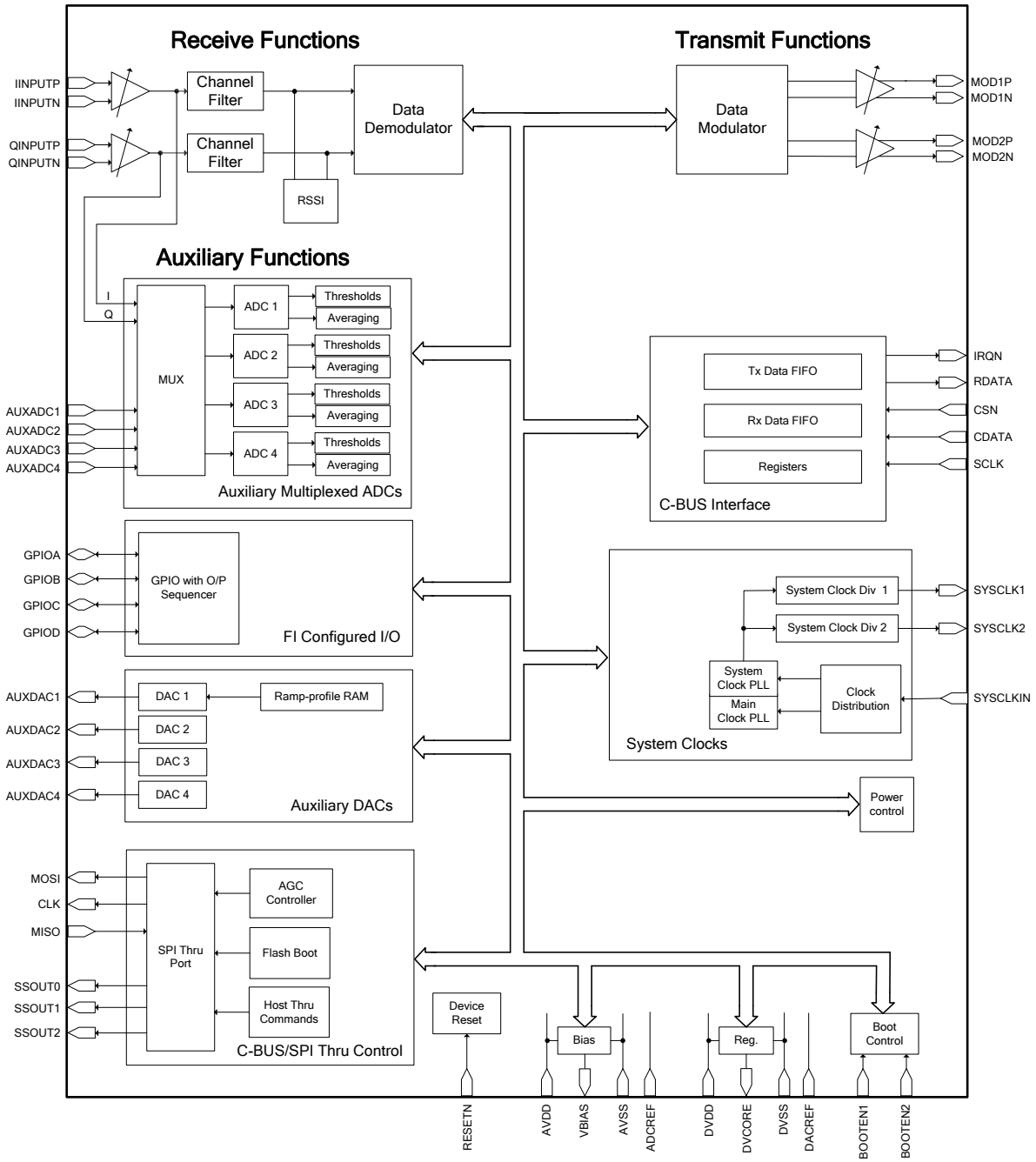


Figure 1 Overall Block Diagram

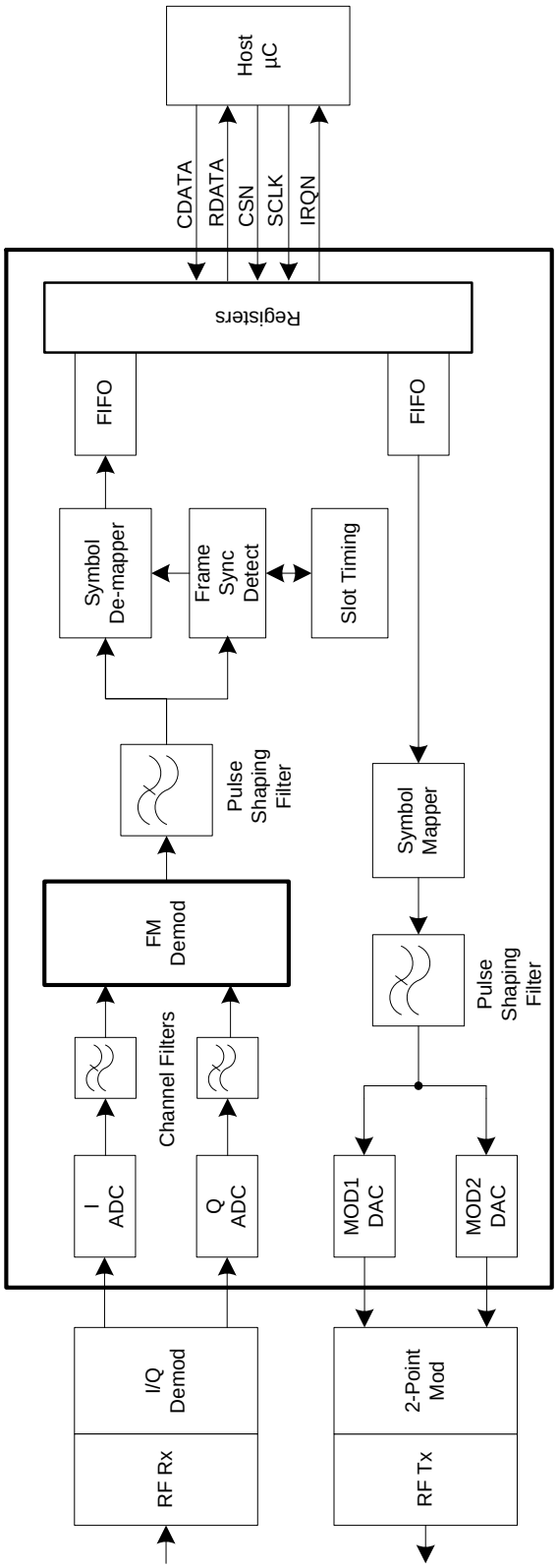


Figure 2 Signal Flow: Two-point Tx with I/Q Rx

3 Signal List

64-pin Q1/L9	Pin		Description
Pin No.	Name	Type	
1	GPIOB	BI	General Purpose I/O (Used as Tx Enable on DE9943)
2	BOOTEN1	IP+PU	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface
3	BOOTEN2	IP+PU	The combined state of BOOTEN1 and BOOTEN2, upon RESET, determine the Function Image™ load interface
4	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
5	DVDD	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DV_{SS} by capacitors mounted close to the supply pins.
6	SSOUT2	OP	SPI: Slave Select Out 2
7	RESETN	IP	Logic input used to reset the device (active low)
8	GPIOC	BI	General Purpose I/O
9	GPIOD	BI	General Purpose I/O
10	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
11	NC	NC	Do not connect
12	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.
13	NC	NC	Do not connect
14	NC	NC	Do not connect
15	NC	NC	Do not connect
16	NC	NC	Do not connect
17	MOD1P	OP	Differential outputs for Mod 1 signals; ‘P’ is positive, ‘N’ is negative. Together these are referred to as Mod 1 Output.
18	MOD1N	OP	
19	MOD2P	OP	Differential outputs for Mod 2 signals; ‘P’ is positive, ‘N’ is negative. Together these are referred to as Mod 2 Output.
20	MOD2N	OP	
21	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits
22	DACREF	~	DAC reference voltage, connect to AV_{SS}
23	NC	NC	Do not connect
24	NC	NC	Do not connect
25	NC	NC	Do not connect
26	NC	NC	Do not connect

64-pin Q1/L9	Pin		Description
Pin No.	Name	Type	
27	VBIAS	OP	Internally generated bias voltage of approximately $AV_{DD}/2$. If V_{BIAS} is powersaved this pin will be connected via a high impedance to AV_{DD}. This pin must be decoupled to AV_{SS} by a capacitor mounted close to the device pins.
28	IINPUTP	IP	Differential inputs for I channel signals; 'P' is positive, 'N' is negative. Together these are referred to as the I Input.
29	IINPUTN	IP	
30	ADCREF	~	ADC reference voltage; connect to AV_{SS}
31	QINPUTP	IP	Differential inputs for Q channel signals; 'P' is positive, 'N' is negative. Together these are referred to as the Q Input.
32	QINPUTN	IP	
33	AUXADC1	IP	Auxiliary ADC input 1
34	AUXADC2	IP	Auxiliary ADC input 2
35	AUXADC3	IP	Auxiliary ADC input 3
36	AUXADC4	IP	Auxiliary ADC input 4
37	AVDD	PWR	Positive 3.3V supply rail for the analogue on-chip circuit. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.
38	AVSS	PWR	Negative supply rail (ground) for the analogue on-chip circuits
39	AUXDAC1	OP	Auxiliary DAC output 1 (Optionally the RAMDAC output)
40	AUXDAC2	OP	Auxiliary DAC output 2
41	AUXDAC3	OP	Auxiliary DAC output 3
42	AUXDAC4	OP	Auxiliary DAC output 4
43	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
44	DVCORE	PWR	Internally generated digital core voltage of approximately 1.8V. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins
45	DVDD	PWR	3.3V positive supply rail for the digital on-chip circuits. This pin should be decoupled to DV_{SS} by capacitors mounted close to the supply pins.
46	NC	NC	Do not connect
47	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
48	DVSS	PWR	Negative supply rail (ground) for the digital on-chip circuits
49	NC	NC	Do not connect
50	SYSCLKIN	IP	Input from the external system clock source
51	SYSCLK1	OP	Synthesised digital clock output 1
52	SYSCLK2	OP	Synthesised digital clock output 2
53	SCLK	IP	C-BUS serial clock input from the µC

64-pin Q1/L9	Pin		Description
Pin No.	Name	Type	
54	RDATA	TS OP	3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
55	CDATA	IP	C-BUS serial data input from the µC
56	CSN	IP	C-BUS chip select input from the µC
57	IRQN	OP	'wire-Orable' output for connection to the Interrupt Request input of the µC. This output is pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor is required.
58	DVCORE	PWR	Internally generated digital core voltage of approximately 1.8V. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins
59	MOSI	OP	SPI: Master Out Slave In
60	SSOUT1	OP	SPI: Slave Select Out 1
61	MISO	IP	SPI: Master In Slave Out
62	SSOUT0	OP	SPI: Slave Select Out 0
63	CLK	OP	SPI: Serial Clock
64	GPIOA	BI	General Purpose I/O (Used as Rx Enable on DE9943)
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on the Q1 package only) may be electrically unconnected or, alternatively, may be connected to Analogue ground (AVss). **No other electrical connection is permitted.**

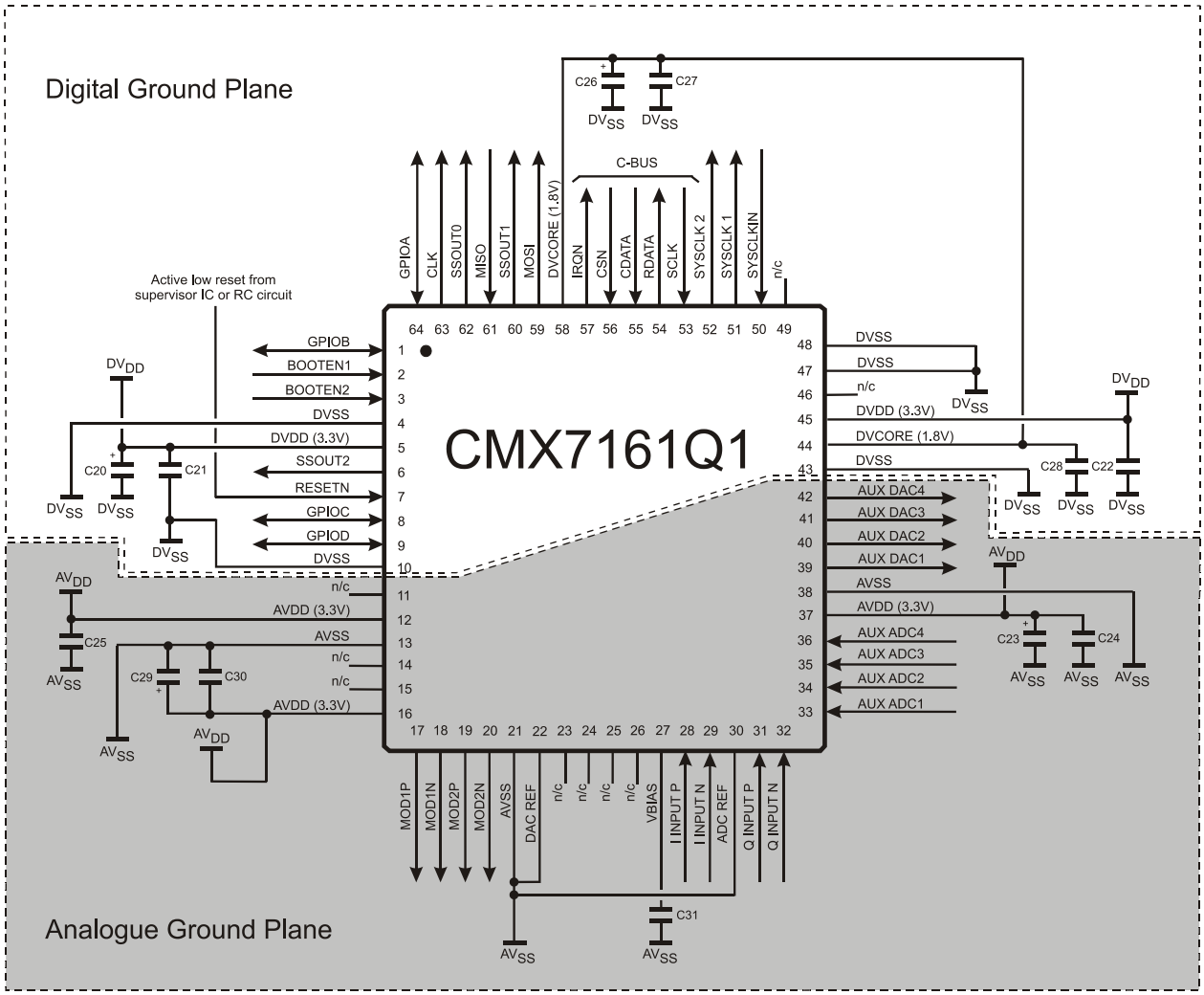
Notes: IP = Input (+ PU/PD = internal pull-up / pull-down resistor of approximately 75kΩ)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
DV_{CORE}	DVCORE	Power supply for core logic, derived from DV_{DD} by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
AV_{SS}	AVSS, SUBSTRATE	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits

4 PCB Layout Guidelines and Power Supply Decoupling



C20	10µF	C26	22µF
C21	10nF	C27	10nF
C22	10nF	C28	10nF
C23	10µF	C29	10µF
C24	10nF	C30	10nF
C25	10nF	C31	100nF

Figure 3 CMX7161 Power Supply and De-coupling

Notes:

To achieve good noise performance, AV_{DD} and V_{BIAS} decoupling and protection of the receive path from extraneous in-band signals is very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX7161 analogue area to provide a low impedance connection between the AVSS pins and the AV_{DD} and V_{BIAS} decoupling capacitors.

5 External Components

5.1 System Clock Interface

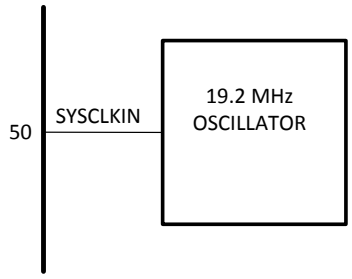
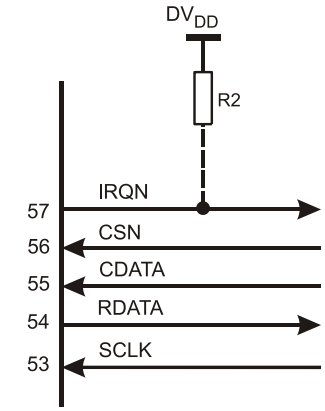


Figure 4 Recommended External Components – System Clock Interface

The system clock circuit is designed to operate with an external oscillator at 19.2 MHz. The external oscillator should be connected to the SYSCLKIN input pin, refer to Figure 3 and Figure 4. For external oscillator frequency range, see Section 8.1, Electrical Performance, Operating Limits. Also refer to Section 7.1.

5.2 C-BUS Interface



R2 10k - 100kΩ

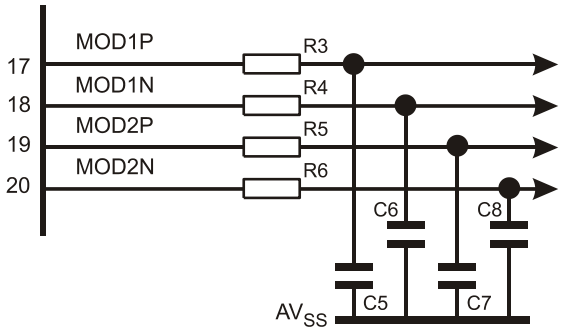
Figure 5 Recommended External Components – C-BUS Interface

Note:

If the IRQN line is connected to other compatible pull-down devices only one pull-up resistor is required on the IRQN node.

5.3 2-point Output Reconstruction Filter

The CMX7161 2-point outputs provide internal reconstruction. To complete the output reconstruction filter the following external RC network (Figure 6) should be used for each of the outputs.



R3-R6 (kOhms)	C5-C8 (pF)
22	270

Figure 6 Recommended External Components – 2-Point Output Reconstruction Filter

5.4 GPIO Pins

By default, after the Function Image™ has been loaded, all GPIO pins are configured as inputs with an internal bus-hold circuit. This avoids the need for users to add external termination (pullup/pulldown) resistors onto these inputs. The bus-hold is equivalent to a 75kΩ resistor either pulling up to logic 1 or pulling down to logic 0. As the input is pulled to the opposite logic state by the user, the bus-hold resistor will change, so that it also pulls to the new logic state. The internal bus-hold can be disabled or re-enabled using the Programming Register.

6 General Description

CMX7161 FI-1.x is a half-duplex digital radio modem intended for use in two-slot TDMA systems such as the ETSI TS 102 361 standard for Digital Mobile Radio (DMR). It uses root-raised-cosine (α=0.2) 4-FSK modulation in a 12.5kHz channel. Slot timing and synchronisation are handled automatically by the device.

An integrated analogue interface supports direct connection to an I/Q receiver and two-point modulation transmitter with few external components; no external codecs are required.

Intelligent auxiliary ADC, DAC and GPIO sub-systems are provided to minimise required host interaction and host I/O resources. Two synthesised system clock generators develop clock signals for off-chip use. The C-BUS/SPI master interface expands host C-BUS/SPI ports to control external devices.

The CMX7161 operates from a 3.3V supply and is available in 64-VQFN and 64-LQFP packages.

The device uses CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™ data file which is uploaded during device initialisation to define the device's function and feature set. The Function Image™ can be loaded automatically from a host µC over the C-BUS serial interface or from an external memory device. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

The device includes provision for an external oscillator, with phase locked loop and buffered output, to provide a System Clock output, if required, for other devices. Block diagrams of the device are shown in Section 2, Block Diagrams.

Tx Functions:

- Two-point modulation analogue outputs
- Root-raised-cosine (α=0.2) pulse shaping
- RAMDAC capability for PA ramping control
- Tx trigger feature allowing precise control of burst start time
- Tx burst sequence for automatic RAMDAC ramping and hardware switching

Rx Functions:

- I/Q analogue inputs
- Rx channel filtering and root-raised-cosine (α=0.2) pulse shaping
- Data returned as hard-decision bits or 4-bit soft-decision LLR metrics
- Automatic frame sync detection simplifies host control
- Automatic tracking of symbol timing and input I/Q DC offsets
- Received Signal Strength Indicator

Slot timing functions:

- 30ms slot format (264-bit bursts)
- Internal slot clock and timing maintenance
- Automatic synchronisation to received channel
- Automatic sequencing of hardware control

Auxiliary Functions:

- Two programmable system clock outputs
- Four auxiliary ADCs with six selectable input paths
- SPI Thru-Port for interfacing to synthesisers and other serially controllable devices
- Four auxiliary DACs, one with built-in programmable RAMDAC
- Tx Enable and Rx Enable

Host Interface:

- Optimised C-BUS (4-wire, high speed synchronous serial command/data bus) interface to host for control and data transfer, including streaming C-BUS for efficient data transfer
- Open drain IRQ to host
- Two GPIO pins
- Serial memory or C-BUS (host) boot mode.

7 Detailed Descriptions

7.1 External Oscillator Frequency

The CMX7161 is designed to work with an external oscillator at 19.2MHz with a frequency tolerance of 0.5ppm.

7.2 Radio Interface

The CMX7161 supports direct connection to a direct conversion receiver such as the CML CMX994 and a two-point modulation transmitter. No external RF codecs are required. An example outline radio design is shown in Figure 7.

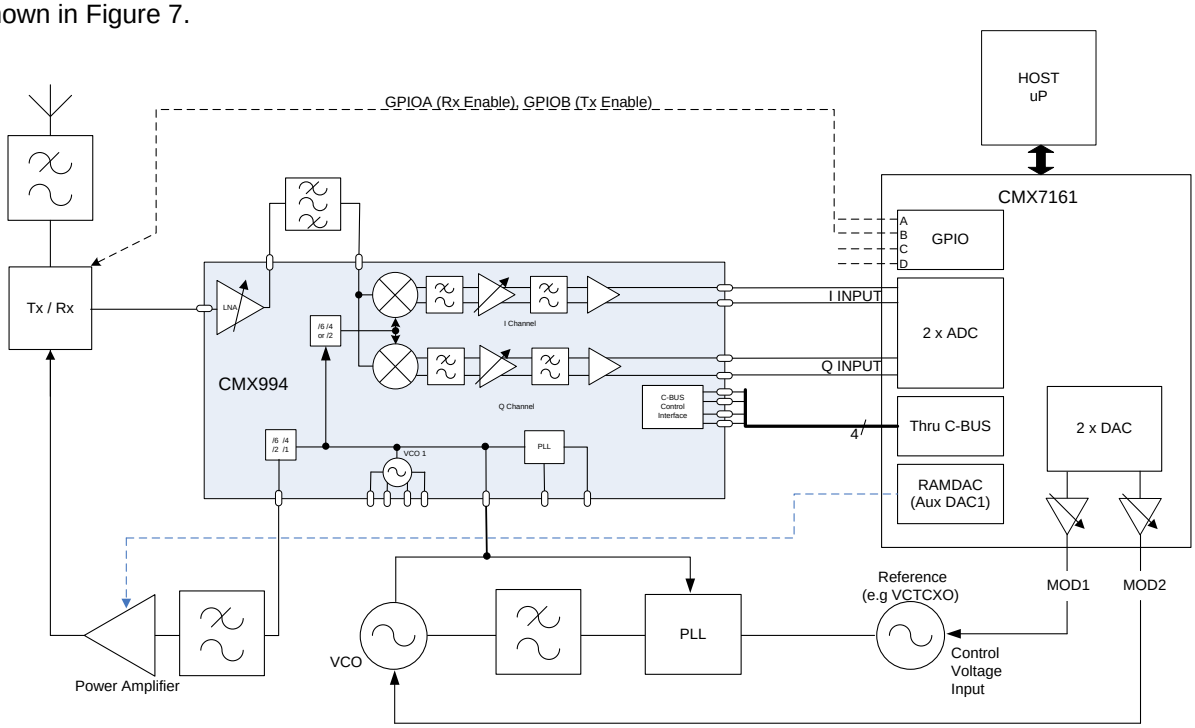


Figure 7 Outline Radio Design

7.3 Host Interface

The primary interface for commands, status information and payload data transfer from the host µC consists of a bank of device registers addressed and accessed using a serial data interface (C-BUS). The C-BUS interface is hardware compatible with Microwire™, SPI™ and other similar interfaces.

A dedicated interrupt line to the host µC is also provided to alert the host µC to significant events. Interrupts of different types can be individually enabled using the IRQ Mask Register ($6C read) and the cause of each interrupt is reported in the IRQ Status Register ($7E read).

7.3.1 C-BUS Operation

C-BUS transactions consist of an address byte sent from the µC followed by zero or more data byte(s) written into or read out from the register that has been addressed. Note that registers are either writable or readable, but not both.

C-BUS registers are 8 or 16 bits wide, and most transactions therefore involve one or two data bytes. Some registers also support streaming transactions in which a single register address byte is followed by many data bytes being written to or read from the CMX7161.

Certain C-BUS transactions require only an address byte to be sent from the µC with no data transfer. This includes the General Reset command.

Data sent from the µC on the CDATA (command data) line is clocked into the CMX7161 on the rising edge of the SCLK input. Data sent from the CMX7161 to the µC on the RDATA (reply data) line is valid when SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

7.3.2 C-BUS Timing

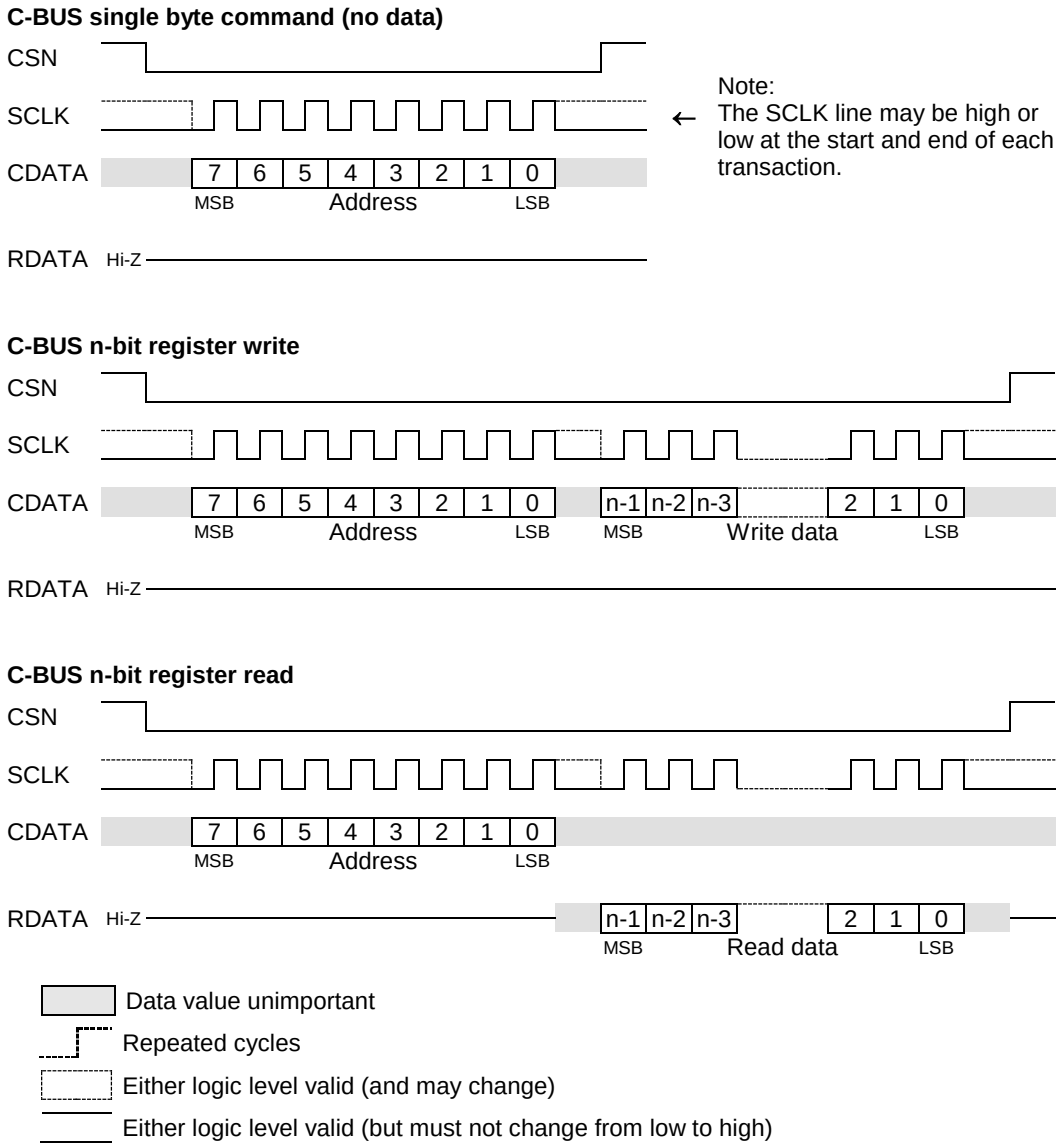
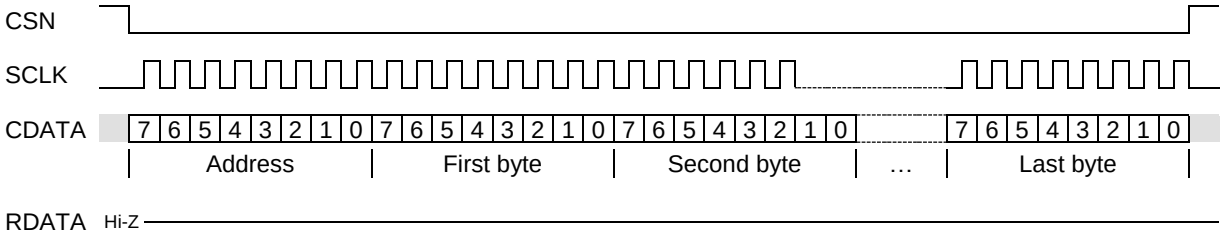


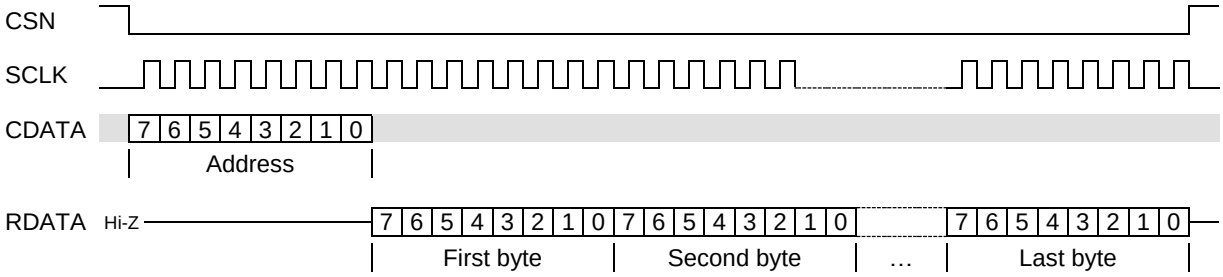
Figure 8 Basic C-BUS Transactions

To reduce overhead some C-BUS read and write registers are capable of streaming operation. This allows multiple read or write data words to follow a single address byte all within the same C-BUS transaction.

C-BUS data-streaming (8-bit write register)



C-BUS data-streaming (8-bit read register)



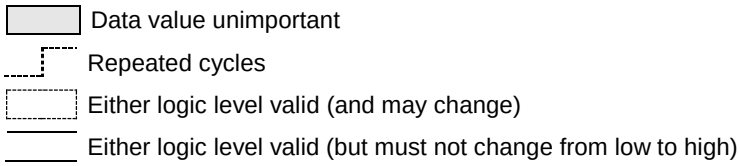


Figure 9 C-BUS Data Streaming Operation

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset)
2. For single byte data transfers only the first 8 bits of the data are transferred
3. The CDATA and RDATA lines are never active at the same time. The address byte determines the data direction for each C-BUS transfer.
4. The SCLK can be high or low at the start and end of each C-BUS transaction
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.4 Function Image™ Loading

The Function Image™ (FI) which defines the operational capabilities of the device may be obtained from the CML Technical Portal, following registration and authorisation. This is a 'C' header file which contains blocks of data to be included with the host controller software or programmed into an external serial memory. The Function Image™ size will never exceed 128 kbytes and a typical FI may be considerably smaller than this. Note that the BOOTEN1/2 pins are only read at power-on, or when the RESETN pin goes high, or following a C-BUS General Reset, and they must remain stable throughout the FI loading process. After an FI load has completed the BOOTEN1/2 pins are ignored by the CMX7161 until the next power-up or Reset.

The BOOTEN1/2 pins are both fitted with internal low current pull-up devices. For serial memory loading BOOTEN2 should be pulled low by connecting it to DV_{SS} either directly or via a 47k resistor (see Table 2).

The boot loader reports back the checksum of each FI data block in the C-BUS Device Information - $4D, read register. These can be read back in sequence and checked against the values provided along with the FI to verify that it has loaded correctly. After the FI has finished loading the CMX7161 will also report its product identification code ($7161) and version code in the Device Information Register.

Once the Function Image™ is loaded and the CMX7161 has fully initialised itself, the Mode bit in the register is set and the device enters Sleep mode by default. The contents of the Device Information Register are valid while the CMX7161 remains in this initial Sleep state but the register should NOT be accessed after any active operating mode has been selected.

If the host detects a brownout, the FI must be reloaded. The BOOTEN1/2 pins should be configured appropriately and a General Reset should then be issued or the RESETN pin used to reset the CMX7161. The appropriate FI load procedure can then be followed.

Table 2 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS host load	1	1
reserved	1	0
Serial Memory load	0	1
reserved	0	0

7.4.1 FI Loading from Host Controller

The Function Image™ can be included with the host controller software for download into the CMX7161 at power-up over the C-BUS interface. This is done by writing the FI data into the FI Load Register ($49 write) which supports streaming operation. The BOOTEN1/2 pins must first be set to the C-BUS load configuration and the CMX7161 then powered up or Reset before the FI data is sent over C-BUS.

Depending on the rate of data transfer by the host, the FI data may be buffered by the device during loading. The Transmit FIFO Level Register ($4B read) indicates the fill level of the FI load FIFO which has a maximum capacity of 128 bytes. This level should be checked to ensure the buffer does not overflow.

Otherwise FI download time is limited only by the clock frequency of the C-BUS. With a 19.2MHz SCLK it should take less than 250ms to complete even when loading the largest possible Function Image™.

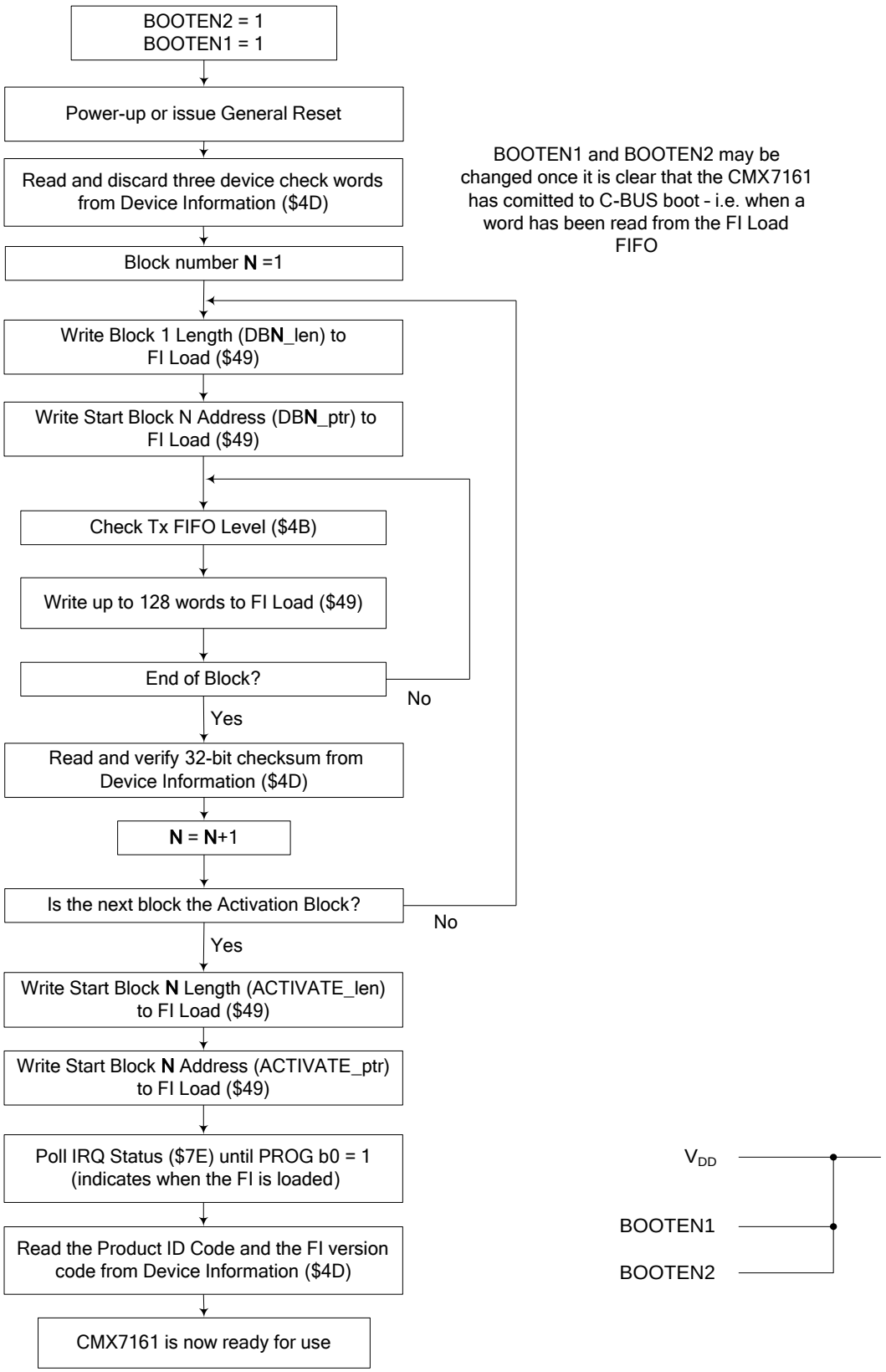


Figure 10 FI Loading from Host

7.4.2 FI Loading from Serial Memory

The Function Image™ should be converted into a suitable format for the serial memory programmer (usually Intel Hex) and then loaded into the serial memory either by the host or an external programmer. The serial memory should contain the data stream written to the FI Load Register shown in Figure 10. The most significant byte of each 16-bit word should be stored first in serial memory.

The serial memory should be interfaced to the CMX7161 SPI Thru-Port using SSOUT0 as the chip select. The CMX7161 needs to have the BOOTEN pins set to Serial Memory Load. The CMX7161 will then automatically load the data from the serial memory without intervention from the host controller at power-on, or following the RESETN pin becoming high, or following a C-BUS General Reset.

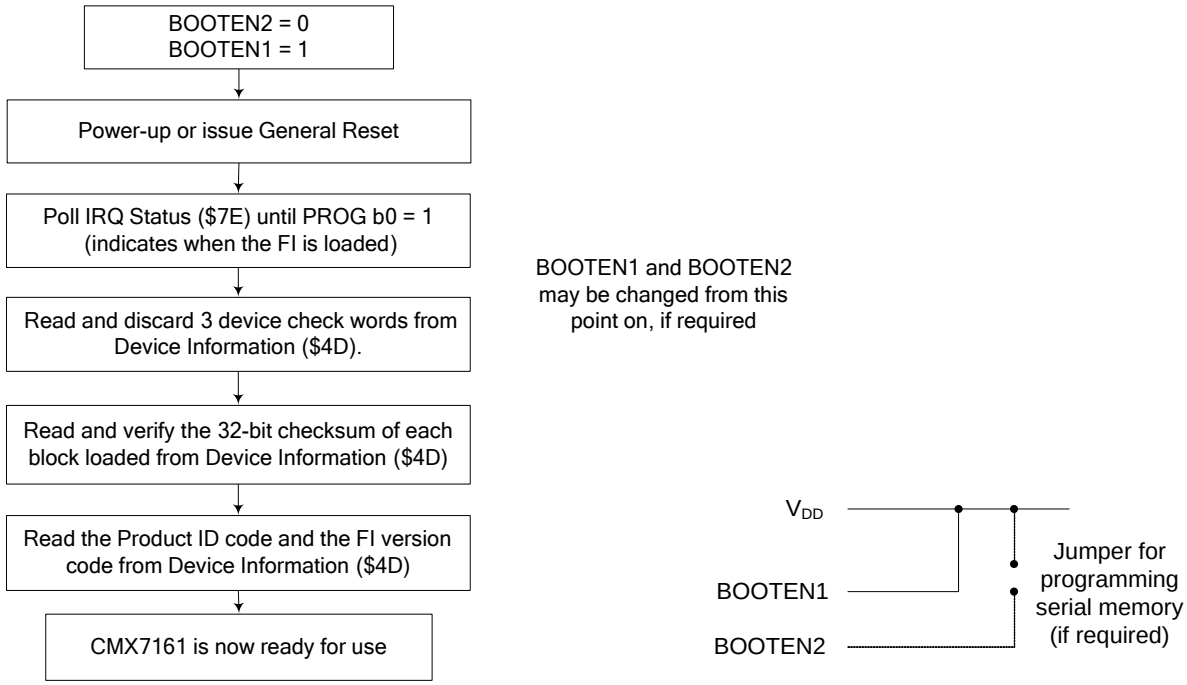


Figure 11 FI Loading from Serial Memory

The CMX7161 has been specifically designed to function with the AT25F512 serial flash device but other manufacturers' parts may also be suitable. The maximum loading time should be less than 500ms even when loading the largest possible Function Image™.

7.5 Device Control

Device control is primarily carried out by writing and reading registers over the C-BUS interface.

7.5.1 Device Control Overview

The CMX7161 can be set into four main operating modes using the Modem Control Register ($6B write):

- Sleep mode – for power saving and device configuration
- Transmit mode – for continuous transmission
- Receive mode – for detection and reception of continuous data
- Slotted mode – for transmission and reception in 30ms slots

To conserve power the device can be placed into Sleep mode when not actively processing a signal. Additional power-saving can be achieved by disabling unused hardware blocks; however most hardware power-saving is automatic by default.

A number of other registers are used to configure the device during operation. While in Sleep mode the Programming Register ($6A write) can also be used to configure device parameters that are changed less frequently.

Payload data is transferred to and from the host via the Transmit and Receive FIFO buffers.

A dedicated interrupt line is provided to alert the host µC to significant events. Interrupt of different types can be individually enabled using the IRQ Mask Register ($6C read) and the cause of each interrupt is reported in the IRQ Status Register ($7E read).

7.5.2 Device Configuration (Programming Register)

The Programming Register ($6A write) gives access to internal device registers which configure device parameters that are changed less frequently. These will normally need to be modified only at power-on or during major mode changes (if at all). They can only be accessed while the device is in Sleep mode.

Full details of how to configure these aspects of device operation are given in the User Manual.

7.5.3 Data Transfer

Payload data is transferred to and from the host via the Transmit and Receive FIFO buffers, which provide efficient streaming C-BUS access to transfer blocks of data with minimal overhead. The FIFOs can be accessed at any time allowing data to be loaded and retrieved when most convenient.

Each FIFO holds a maximum of 128 bytes of data. Current fill-levels can be determined by reading the Transmit and Receive FIFO Level Registers ($4B, $4F read). The FIFO Control Register ($50 write) can be used to set fill-level thresholds which will generate host interrupts on being reached.

7.5.4 Interrupt Operation

The CMX7161 can produce an interrupt output when various events occur such as detection of a frame synchronisation word or a FIFO threshold being reached.

Each event has an associated IRQ Status register bit and an IRQ Mask register bit. The IRQ Mask register is used to select which status events will trigger an interrupt on the IRQN line. All events can be masked using the IRQ mask bit (bit 15) or individually masked using the IRQ Mask register. Enabling an interrupt by setting a mask bit (0→1) after the corresponding IRQ Status register bit has already been set to 1 will also cause an interrupt on the IRQN line. The IRQ bit (bit 15) of the IRQ Status register reflects the IRQN line state.

All interrupt flag bits in the IRQ Status register are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. See:

- IRQ Status - $7E, read
- IRQ Mask - $6C, write

7.5.5 Signal Control

The CMX7161 offers two signal inputs (I Input, Q Input), and two modulator outputs (Mod 1 Output, Mod 2 Output). The analogue gain/attenuation of each input and output can be set individually.

During transmission the device outputs the filtered symbol stream on both Mod 1 and Mod 2. These can then be used to drive VCOs in order to create FM modulation. The two outputs can be independently controlled (gain, offset, polarity).

In receive mode the I and Q inputs accept in-phase and quadrature signals, and may be independently inverted. (Note that inverting one of the inputs has the same effect as swapping the I and Q signals.)

Use of I/Q receive mode brings with it the problem of I/Q DC offsets. These are DC offsets caused by the radio receiver, resulting in the signal into the CMX7161 having a DC offset other than V_{BIAS}. This offset needs to be removed prior to demodulation. Offsets typically remain constant for a particular radio frequency selected, but may vary if that frequency is changed. Gain within the radio receiver may also affect the DC offset seen by the CMX7161.

I/Q DC offset effects are a radio issue which is beyond the control of the CMX7161 but the device does provide DC offset calculation and removal. The host can set DC offset for each input and either lock them or allow the CMX7161 to track them, in which case the updated offsets can be read back later if required.

7.6 Modulation Format

The CMX7161 uses 4-FSK modulation running at 4800 symbols/s (9600bits/s) with a deviation index of 0.27 for transmission in a 12.5kHz channel bandwidth. The symbol stream is converted to a series of impulses which pass through a root-raised-cosine (α=0.2) pulse shaping filter before frequency modulation at the transmitter and again after frequency demodulation at the receiver. The bit-to-symbol mapping is shown below:

Bit Pair	Symbol	Deviation
01	+3	+1944Hz
00	+1	+648Hz
10	-1	-648Hz
11	-3	-1944Hz

7.6.1 Typical Transmit Performance

Using the test system shown in Figure 12 the CMX7161 internal PRBS generator was used to modulate the RF FM signal generator. Some typical results are shown in Figure 13. The desired deviation was achieved by adjusting the deviation control on the RF signal generator.

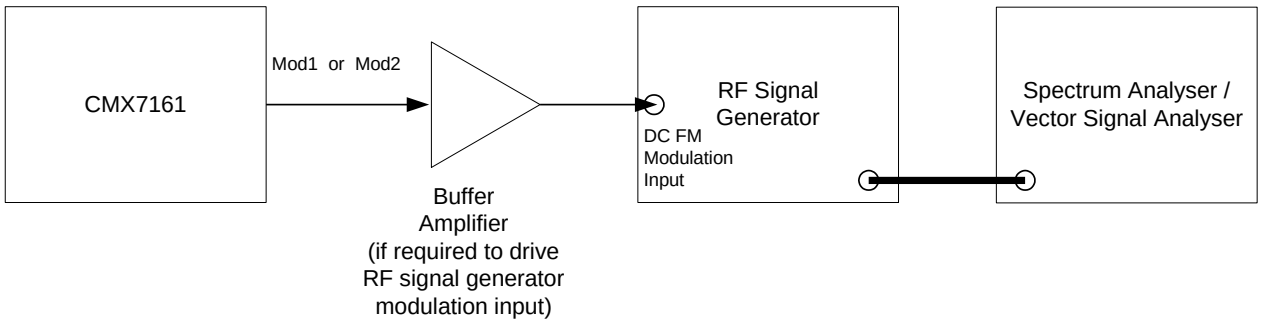


Figure 12 Tx Spectrum and Modulation Measurement Configuration for Two-point Modulation

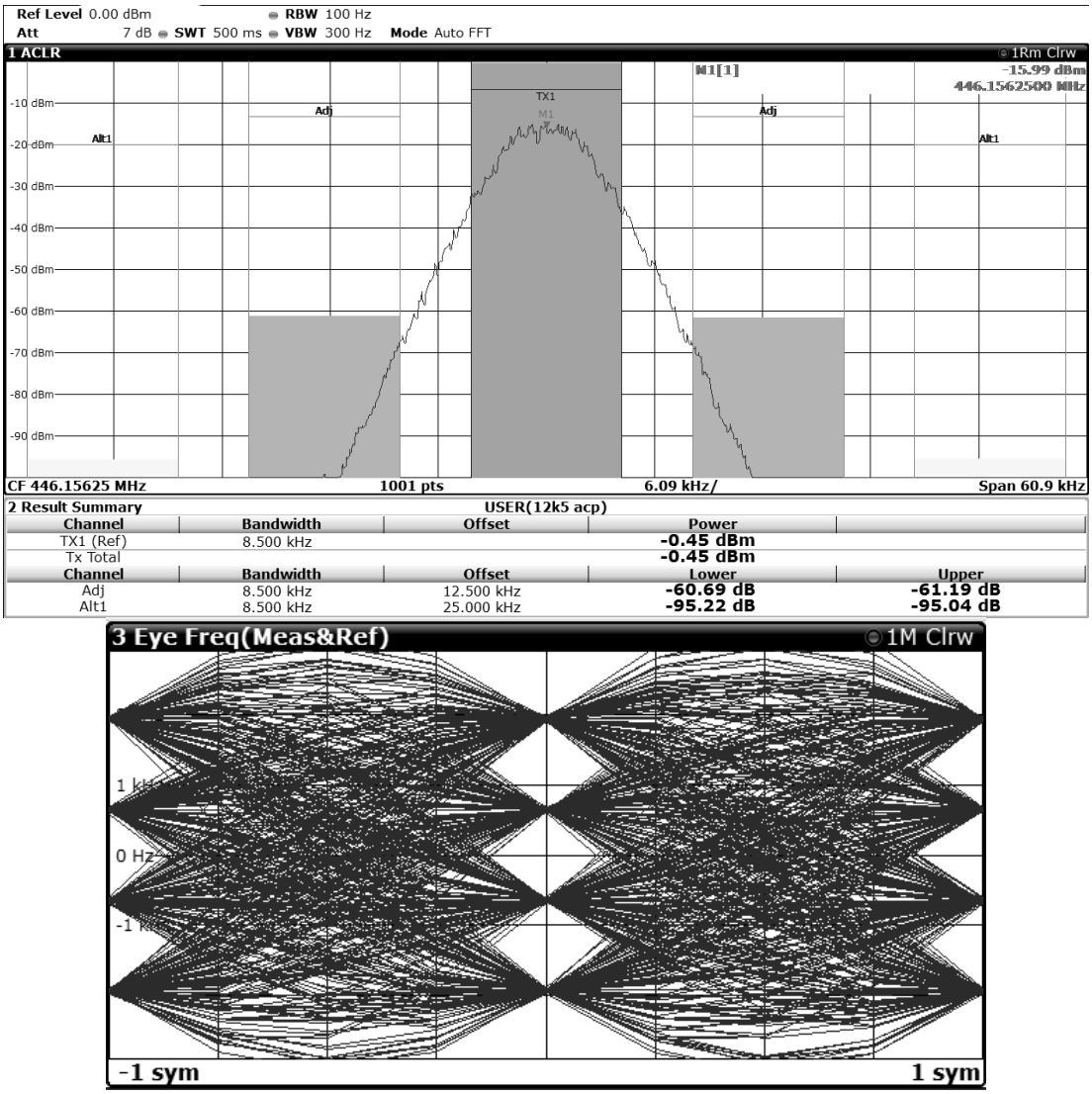


Figure 13 Tx Modulation Spectra (4-FSK, 9.6kbps, RRC – 0.2)

7.7 Slot Structure and Frame Synchronisation

A two-slot TDMA structure is supported. Each slot is 30ms in length comprising a 27.5ms data burst with 2.5ms of guard time. Each data burst contains 216 bits of payload data in two 108-bit blocks, with a central 48-bit field which may contain either a frame synchronisation word or embedded signalling data. The entire contents of each burst (264 bits) are always transferred to/from the host regardless of the contents of the central field.

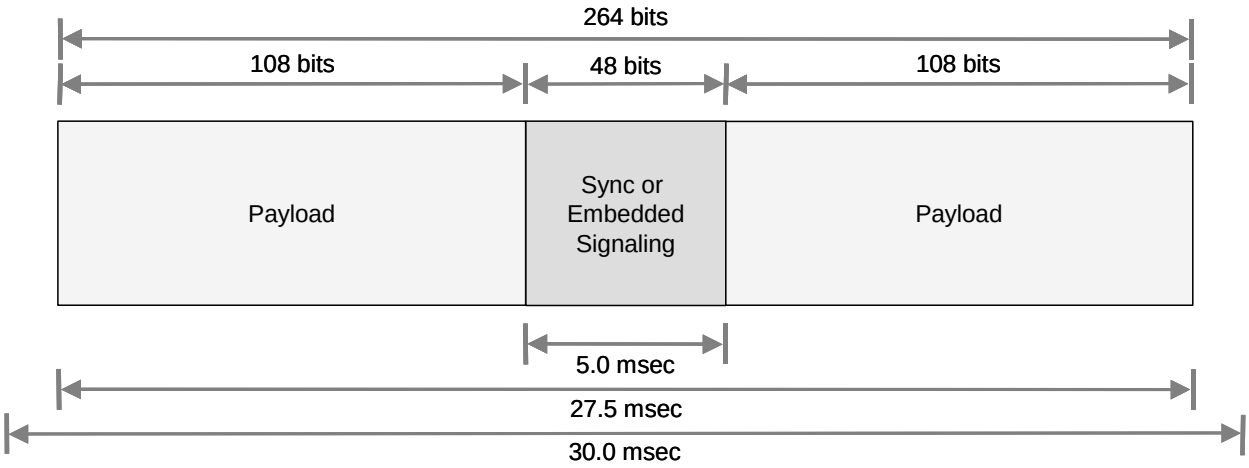


Figure 14 Slot Structure

When searching for frame synchronisation CMX7161 is able to scan for any combination of the ten synchronisation words defined by TS 102 361 by setting the appropriate bits in the Modem Options - $69, write register. In order to acquire system slot timing from a received signal an initial frame sync is required. However once slot timing has been established the CMX7161 will maintain its own internal slot and symbol timing reference, allowing it to receive data bursts in slots that do not contain a synchronisation word.

$755FD7DF75F7	FS0: BS voice
$DFF57D75DF5D	FS1: BS data
$7F7D5DD57DFD	FS2: MS voice
$D5D7F77FD757	FS3: MS data
$77D55F7DFD77	FS4: MS reverse channel
$5D577F7757FF	FS5: TDMA direct slot 1 voice
$F7FDD5DDFD55	FS6: TDMA direct slot 1 data
$7DFFD5F55D5F	FS7: TDMA direct slot 2 voice
$D7557F5FF7F5	FS8: TDMA direct slot 2 data
$DD7FF5D757DD	FS9: (reserved)

The CMX7161 transmit burst timing is linked directly to timing of the received synchronisation word. The timing may be adjusted by timing parameters that can be accessed via the programming registers (P2.x), Timing relationships between the various signals are shown in Figure 15, referring to the figure the following parameters apply as follows:

A = value set in P2.0
B = value set in P2.1
C = value set in P2.2
D = valve set in P2.3
E = constant offset between received synchronisation word and internal timing reference.

The value programmed in each register has a resolution of 1/480 µs, e.g. $C0 = 192 (decimal) = 0.4 ms.

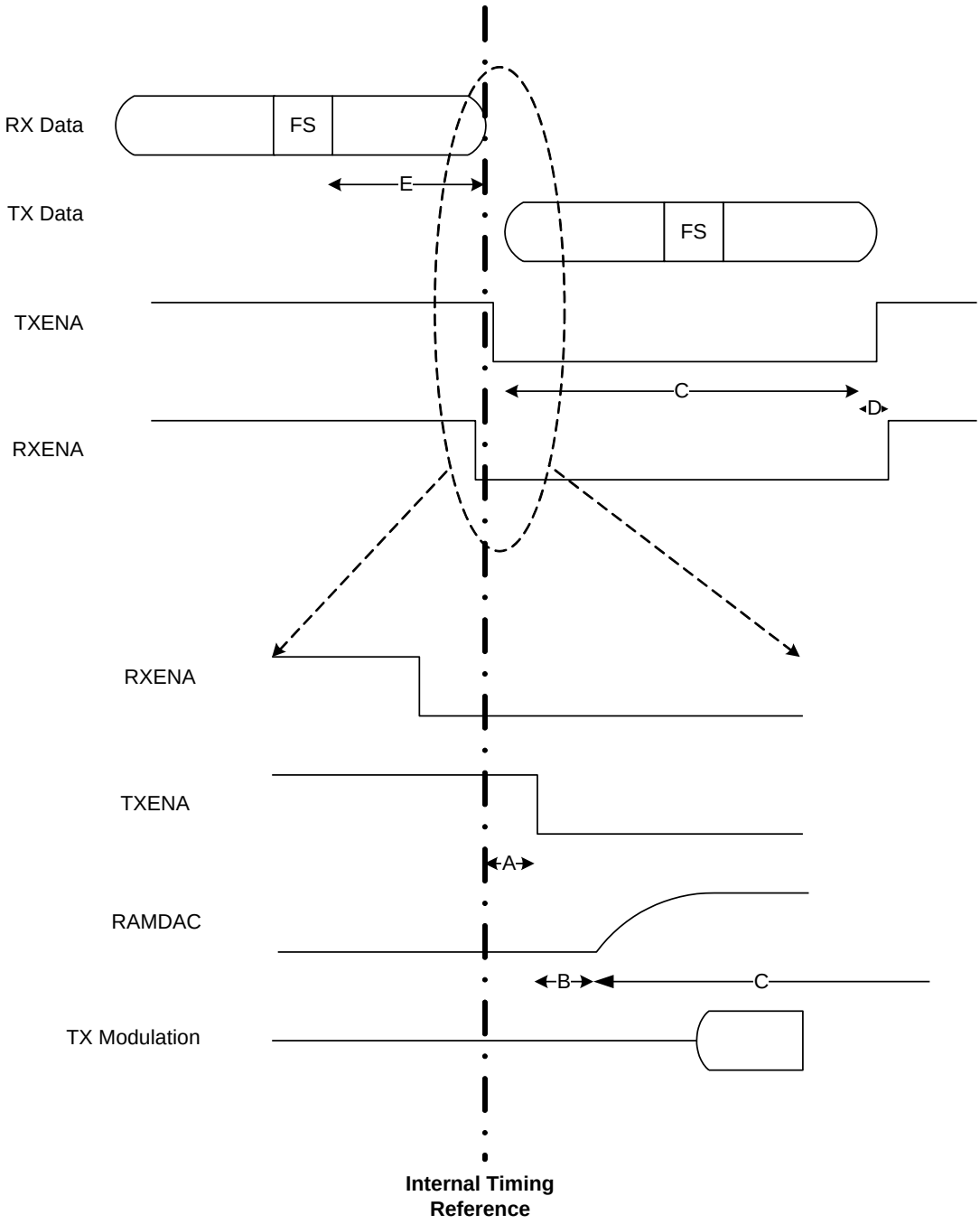


Figure 15 Timing relationships

7.8 Operating Modes

The CMX7161 can be set into four main operating modes using the Modem Control - $6B, write register:

- Sleep mode – for power saving and device configuration
- Transmit Data mode – for continuous transmission
- Receive Data mode – for continuous reception
- Slotted Data mode – for transmission and reception in 30ms slots

A number of test modes are also provided for set-up and calibration.

7.8.1 Sleep Mode (0000)
Sleep mode is the device's lowest power state. While in Sleep mode the Programming - $6A, write register is available to configure device parameters.

7.8.2 Tx Set-up Mode (1001)
A repeating data sequence is modulated and sent continuously. The data sequence can be selected using bits 5-4 of the Modem Control Register ($6B) from:

- $5F repeating (for Tx calibration as specified by TS 102 361)
- $55 $55 $55 $55 $FF $FF $FF $FF (sixteen +3 symbols, sixteen -3 symbols)
- $55 repeating (continuous +3 symbols)
- $7F $7D $5D $D5 $7D $FD (MS Voice frame sync pattern)

7.8.3 Tx PRBS Mode (1010)
A repeating 511-bit PRBS (pseudo random bit sequence) conforming to ITU-T O.153 (Paragraph 2.1) is modulated and sent continuously.

7.8.4 Tx Data Mode (1011)
Data loaded by the host into the Transmit FIFO is modulated and sent continuously. Data can be preloaded into the FIFO before setting the device into Tx Data Mode, if required. The host should ensure that the FIFO does not run empty during transmission.

7.8.5 Rx Set-up Mode (0001)
The received I/Q signals are output on the MOD 1 and 2 outputs with DC offsets and gains applied.

7.8.6 Rx Eye Mode (0010)
The received I/Q signals are channel filtered, demodulated and root-raised-cosine filtered. The resulting baseband signal is output on MOD 1 along with a symbol-rate clock pulse on MOD 2. These outputs can be used to generate an eye diagram on a suitable oscilloscope. Note that the clock pulse is generated locally and is not derived from the input signal.

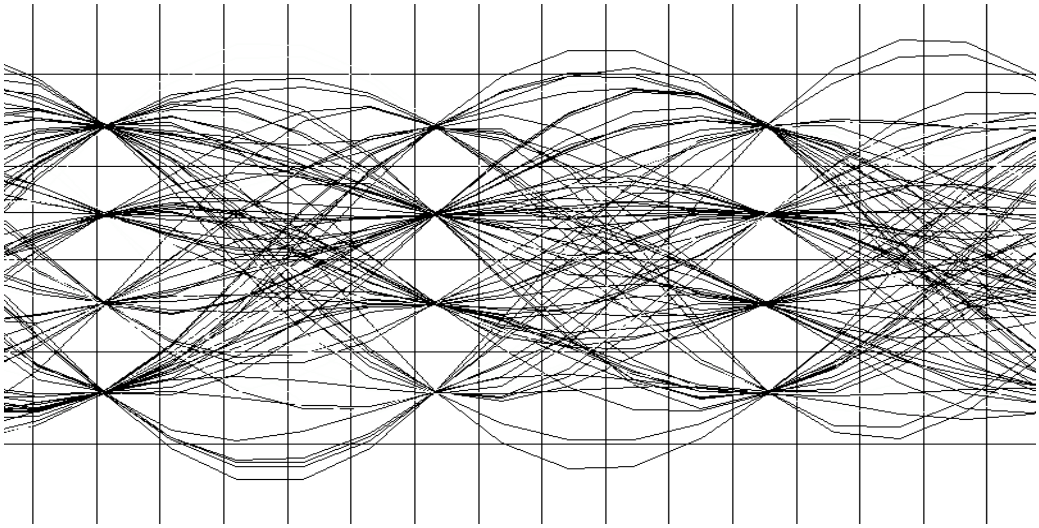


Figure 16 Received Eye Diagram

7.8.7 Rx Data Mode (0011)
The received I/Q signals are channel filtered, demodulated and root-raised-cosine filtered. The CMX7161 initially scans for frame synchronisation according to the frame syncs selected in the Modem Options - $69, write register. When a valid frame sync is detected, a Sync interrupt is issued, the detected sync word is reported in the Receive Status - $7A, read register and the CMX7161 begins demodulating data which is returned to the host via the Receive FIFO - $4C, streaming read register, including the frame sync and the 108 preceding bits. Data is returned either as hard-decision bits or as 4-bit soft-decision LLR metrics

depending on the setting in the Modem Options - $69, write register. The CMX7161 continues to receive data until another mode is selected, or Rx Data mode is re-written to the Modem Control register to restart frame sync search.

7.8.8 Slotted Data Mode (1111)

In slotted mode operation, a two-slot TDMA structure is supported with slots. Each 30ms slot can be designated a receive, transmit or idle slot using the upper byte of the Modem Control register. Data from Receive slots is returned via the register, and data for Transmit slots should be loaded via the Transmit FIFO - $48, streaming write register. All 264 bits in each burst are transferred including the frame sync / signalling bits. Received data can be returned to the host either as hard-decision bits or as 4-bit soft-decision log likelihood ratio (LLR) metrics.

Slot timing can be established from the received signal (using received frame syncs as the reference) or from a local reference (i.e. the host). Once the slot timing has been established the CMX7161 will maintain its own internal slot clock using corrections from received bursts where available. The host can adjust transmit timing in either slot using the Slot Control - $68, write register.

A host IRQ is issued for each slot as a timing reference and to indicate when data should be loaded for Transmit slots. If a local slot timing reference is in use the CMX7161 a GPIO pin can be configured as slot timing input or the CMX7161 can begin transmission immediately on command. A GPIO can also optionally be designated as a slot timing output reference.

7.9 Signal Level Optimisation

The internal signal processing of the CMX7161 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V supply the signal range which can be accommodated without distortion is specified in 8.1.3 Operating Characteristics. Signal gain and DC offset can be manipulated as follows:

7.9.1 Transmit Path Levels

The Coarse Output Gain setting has a range of +6dB to –14.2dB in 0.2dB steps. The Fine Output Gain setting can be used to achieve precise control.

The Mod 1 and Mod 2 outputs may be independently inverted by setting negative Fine Output Gain values.

DC offsets may also be applied to each output, but care must be taken that the combination of gain settings and DC offset do not cause the signal to clip at any point in the processing sequence. The order of processing is Fine Gain, followed by DC offset, followed by Coarse Gain.

See also:

- Mod 2/1 Output Control - $5D, $5E, write
- Mod 1/2 Output Power Control - $B3, write
- Mod 1/2 Output Coarse Gain - $B4, $B5 write

7.9.2 Receive Path Levels

The Coarse Input Gain setting has a range of 0dB to +22.4.dB in 3.2dB steps

When receiving I/Q format signals, inverting one of the I/Q pair has a similar effect to swapping I with Q.

DC offsets can be removed by the CMX7161: the offset to remove can be specified by the host or calculated automatically by the CMX7161. It should be noted that if the maximum allowable signal input level is exceeded, signal distortion will occur regardless of the internal DC offset removal.

See also:

- I/Q Input Control - $5F, $60 write
- I/Q Input Power Control - $B0, write
- I/Q Input Coarse Gain - $B1, $B2 write

7.10 External Interfaces

The CMX7161 provides additional external interfaces to assist with controlling the radio transmitter and receiver. These include:

- Four auxiliary ADCs
- Four auxiliary DACs, one of which may be configured as a RAMDAC to control PA ramping
- An SPI Thru-Port port which may be used to control radio ICs with C-BUS/SPI interfaces
- Four GPIO pins which may be used for Tx/Rx switching, LNA off and general device control.

7.10.1 GPIO Pin Operation

The CMX7161 provides four GPIO pins, each of which can be configured independently as automatic/manual, input/output and rising/falling (with the exception of the combination automatic + input function which is only allowed for GPIOA).

Pins that are automatic outputs become part of a transmit sequence and will automatically switch, along with the RAMDAC – AuxDAC1 (if it is configured as automatic), during the course of a burst. Pins that are manual are under direct user control. When automatic, a rising or a falling event at the start or end of transmission will cause the specified GPIO to be switched high or low accordingly.

GPIOA may be configured as an automatic input. This means that any attempted transmission will wait until GPIOA input is high (if rising is selected) or low (if falling is selected).

Note: On the DE9943 Evaluation Kit, GPIOB is used as Tx Enable; GPIOA is used as Rx Enable.

See:

- GPIO Control - $64, write
- GPIO Input - $79, read.

7.10.2 Auxiliary ADC Operation

The inputs to the four Auxiliary ADCs can be independently routed from any of four dedicated AuxADC input pins or from the two main I/Q inputs. If not required the AuxADCs can be disabled to save power. BIAS in the VBIAS Control - $B7, write register must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC1-4 Control - $51 to $54, write registers. This is a rolling average in which a proportion of the current sample is combined at each step with the previous average value. The proportion is determined by the value of the average counter in the AuxADC1-4 Control - $51 to $54, write registers. Setting the average counter to zero disables the averager; an value of 1 means that 50% of the current sample will be applied; a value of 2 gives 25%, 3 gives 12.5%, continuing up to the maximum useful value of 11 giving 0.0488%.

High and low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when an input exceeds the high or low threshold, or on every sample as required. The thresholds are programmed via the AuxADC1-4 Threshold - $55 to $58, write register.

Auxiliary ADC data is read back in the AuxADC1-4 Read - $71 to $74, read registers and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

The AuxADC sample rate is selected using:

- AuxADC1-4 Control - $51 to $54, write
- AuxADC1-4 Threshold - $55 to $58, write
- AuxADC1-4 Read - $71 to $74, read
- V_{BIAS} Control - $B7, write.

7.10.3 Auxiliary DAC/RAMDAC Operation

The four auxiliary DACs are programmed via the AuxDAC1-4 Control - $59 to $5C, write registers. AuxDAC1 may also be programmed to operate as a RAMDAC which will autonomously output a pre-programmed profile at a programmed rate. The AuxDAC1-4 Control - $59 to $5C, write register, with b14 set, controls the RAMDAC mode of operation when configured as a manually triggered RAMDAC.

The default profile is a Raised Cosine (see Table 5 in the user manual), but this may be over-written with a user defined profile by writing to Program Block 0. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero.

See:

- AuxDAC1-4 Control - $59 to $5C, write
- Program Block 0 - RAMDAC
- Program Block 1 – Clock Control

7.10.4 SPI Thru-Port

The CMX7161 offers an SPI Thru-Port which allows the host, using the main C-BUS interface, to command the CMX7161 to read or write up to three external SPI/C-BUS devices attached to the CMX7161. The CMX7161 acts as an SPI/C-BUS master in this mode, controlling three chip selects, clock and data out (MOSI), and receiving data in (MISO).

The port can be independently configured for each chip select with clock speed, inter-frame guard period and clock phase/polarity to match the specification of the slave SPI/C-BUS device attached. The port can be used for C-BUS operation or in raw SPI mode. In C-BUS mode the data read/written is assumed to be in the format:

Address byte, data byte 1 (optional), data byte 2 (optional)

The CMX7161, as the master, drives both the address and data for write operations. For read operations it drives the address and receives the data. Transactions may carry 0, 1 or 2 bytes of data (a zero-byte write typically being a reset command).

SPI mode is more flexible. No assumption is made about the SPI word format, nor any assumption that the length is a whole number of bytes.

See:

- SPI Thru-Port Control - $62, write
- SPI Thru-Port Write - $63, write
- SPI Thru-Port Read - $78, read

7.11 Digital System Clock Generators

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits as required. The System Clock circuitry is shown in Figure 17 Digital System Clock Generation Schemes.

Having chosen the input frequency source, system clock generation may be done by simply dividing the input frequency source, or via its own phase locked loop. The system clock PLL does not affect any other internal operation of the CMX7161 – so if a frequency that is not a simple fraction of the external oscillator frequency is required, it can be used with no side effects. There is one phase locked loop, with independent output dividers to provide phase locked output signals.

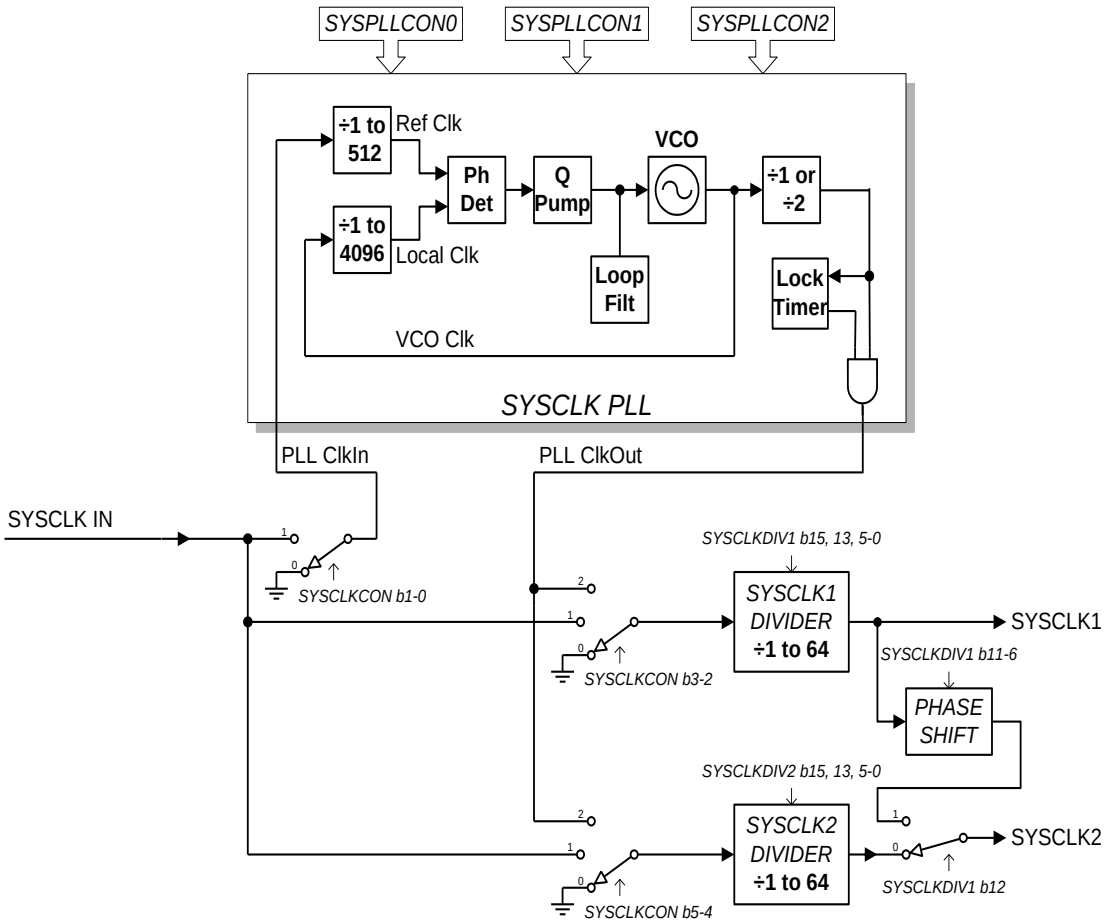


Figure 17 Digital System Clock Generation Schemes

See:

- Program Block 1 – Clock Control

7.12 C-BUS Register Summary

Table 3 C-BUS Registers

ADDR. (hex)	READ/ WRITE	REGISTER	Word Size (bits)
$01	W	C-BUS General Reset	0
$48	W	Transmit FIFO	8
$49	W	FI Load FIFO	16
$4B	R	Transmit FIFO Level	8
$4C	R	Receive FIFO	8
$4D	R	Device Information	16
$4F	R	Receive FIFO Level	8
$50	W	FIFO Control	16
$51 to $54	W	AuxADC1-4 Control	16
$55 to $58	W	AuxADC1-4 Threshold	16
$59 to $5C	W	AuxDAC1-4 Control	16
$71 to $74	R	AuxADC1-4 Read	16
$5D	W	Mod 2 Output Control	16
$5E	W	Mod 1 Output Control	16
$5F	W	I Input Control	16
$60	W	Q Input Control	16
$75	R	I Input Control Readback	16
$76	R	Q Input Control Readback	16
$7A	R	Receive Status	16
$7B	R	Frequency Error	16
$62	W	SPI Thru-Port Control	16
$63	W	SPI Thru-Port Write	16
$64	W	GPIO Control	16
$77	R	RSSI Value	16
$78	R	SPI Thru-Port Read	16
$79	R	GPIO Input	16
$68	W	Slot Control	16
$69	W	Modem Options	16
$6A	W	Programming	16
$6B	W	Modem Control	16
$6C	W	IRQ Mask	16
$7E	R	IRQ Status	16
$7F	R	Modem Control Readback	16
$B0	W	I/Q Input Power Control	16
$B1	W	I Input Coarse Gain	16
$B2	W	Q Input Coarse Gain	16
$B3	W	Mod 1/2 Output Power Control	16
$B4	W	Mod 1 Output Coarse Gain	16
$B5	W	Mod 2 Output Coarse Gain	16
$B7	W	V_{BIAS} Control	16

All other C-BUS addresses are reserved and must not be accessed.

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Power Supplies			
DV_{DD} - DV_{SS}	-0.3	4.0	V
DV_{CORE} - DV_{SS}	-0.3	2.16	V
AV_{DD} - AV_{SS}	-0.3	4.0	V
Voltage on any pin to V_{SS}	-0.3	IOV_{DD} + 0.3	V

L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at T_{AMB} = 25ºC		1690	mW
... Derating		16.9	mW/ºC
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	ºC

Q1 Package (64-lead VQFN)	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at T_{AMB} = 25ºC		3500	mW
... Derating		35.0	mW/ºC
Storage Temperature	-55	+125	ºC
Operating Temperature	-40	+85	ºC

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Min	Typ	Max.	Units
DV_{DD} - DV_{SS}	3.0	3.3	3.6	V
DV_{CORE} - DV_{SS}	1.7	1.8	1.9	V
AV_{DD} - AV_{SS}	3.0	3.3	3.6	V
Operating Temperature	-40	–	+85	°C
External Clock Frequency	3.0	–	19.2	MHz

8.1.3 Operating Characteristics

Details in this section represent design target values and are not currently guaranteed.

For the following conditions unless otherwise specified:

External components as recommended in Section 5, External Components.
Maximum load on digital outputs = 30pF
T_{AMB} = −40°C to +85°C
AV_{DD} = DV_{DD} = 3.0V to 3.6V

Current consumption figures quoted in this section apply to the device when loaded with FI-1 only. Current consumption may vary with other valid Function Images™.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current (see also section 8.1.4)	11				
All Powersaved					
AI_{DD} + DI_{DD}	10,15	–	1.0	–	µA
Additional current for one auxiliary System Clock (output running at 5MHz – SYSCLKPLL active)	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	900	–	µA
Additional current for one auxiliary System clock (output running at 4.8MHz – SYSCLKPLL not required)	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	675	–	µA
Additional current for each auxiliary ADC	15				
DI_{DD} (DV_{DD} = 3.3V, DV_{CORE} = 1.8V)		–	190	–	µA
Additional current for each auxiliary DAC	14,15				
AI_{DD} (AV_{DD} = 3.3V)		–	210 to 370	–	µA

Notes:

11 T_{AMB} = 25°C, not including any current drawn from the device pins by external circuitry.
12 System Clocks, Auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled and V_{BIAS} enabled.
13 Using a 19.2MHz external clock input.
14 A lower current is measured when outputting the smallest possible dc level from an AuxDAC, a higher current is measured when outputting the largest possible dc value.
15 Using a 19.2MHz external clock input.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
CLK	20				
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic '1'		70%	–	–	DV_{DD}
Input Logic '0'		–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')	11	–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic '1' (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic '0' (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current	11	-1.0	–	1.0	µA
V_{BIAS}	21				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	50	–	kΩ

Notes:

20 Characteristics when driving the SYSCLKIN pin with an external clock source.

21 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor, as shown in Section 4 PCB Layout Guidelines and Power Supply Decoupling.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
CLK Input						
'High' Pulse Width		30	15	–	–	ns
'Low' Pulse Width		30	15	–	–	ns
Input Impedance (at 9.6MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
SYSCLK1/2 Outputs						
SYSPLL Operating Frequency			38	–	250	MHz
SYSCLK1/2 Output Frequency			–	–	20	MHz
Rise Time			–	–	13.5	ns
Fall Time			–	–	6	ns
V_{BIAS}						
Start-up Time (from powersave)			–	30	–	ms
Differential I and Q Inputs						
Input Impedance, Enabled		31	10	–	140	kΩ
Input Impedance, Muted or Powersaved				200		kΩ
Maximum Input Voltage Excursion		32	–	–	20 to 80	%AV_{DD}
Programmable Input Gain Stage						
Gain (at 0dB)		33	−0.5	0	+0.5	dB
Cumulative Gain Error (w.r.t. attenuation at 0dB)		33	−1.0	0	+1.0	dB

Notes:

30 Timing for an external input to the SYSCLKIN pin.

31 With no external components connected.

32 For each input pin and for AV_{DD} = 3.3V, the maximum allowed signal swing is: (3.3 x 0.8) - (3.3 x 0.2) = 2.0V.

33 Design Value. Overall attenuation input to output has a design tolerance of 0dB ±1.0dB.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
Modulator Outputs						
Power-up to Output Stable		40	–	50	100	µs
Output Coarse Gain Attenuators						
Attenuation (at 0dB)		42	–0.2	0	+0.2	dB
Cumulative Attenuation Error (w.r.t. attenuation at 0dB)		42	–0.6	0	+0.6	dB
Output Impedance	Enabled	41	–	600	–	Ω
	Disabled	41	–	TBD	–	kΩ
Output Voltage Range		43, 44	0.3	–	AV_{DD}-0.3	V
Load Resistance			20	–	–	kΩ

Notes:

40 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the C-BUS interface, to be in placed in powersave mode.

41 Small signal impedance, at AV_{DD} = 3.3V and T_{AMB} = 25°C.

42 Figures relate to attenuator block only. Design Value. Overall attenuation input to output has a design tolerance of 0dB ±1.0dB.

43 For each output pin. With respect to the output driving a 20kΩ load to $AV_{DD}/2$.

44 The levels of the MOD2/1 Output Fine Gain and Offsets (registers $5D and $5E) should be adjusted so that the output voltage remains between 20% and 80% of AV_{DD} on each output pin (when 0dB of coarse output gain is used). This will produce the best performance when the device operates with AV_{DD} = 3.3V.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (AuxADC1-4)					
Source Output Impedance	50	–	–	24	kΩ
Auxiliary 10-Bit ADCs					
Resolution		–	10	–	Bits
Conversion Time	51	–	225	–	µs
Sample Rate		1	-	512	Hz
Input Impedance					
Resistance		–	TBD	–	MΩ
Capacitance		–	5	–	pF
Offset Error	54, 55	–	–	±18	mV
Integral Non-linearity	54, 55	–	–	±2	LSBs
Differential Non-linearity	52, 54	–	–	±1	LSBs
Auxiliary 10-Bit DACs					
Resolution		–	10	–	Bits
Conversion Time	51		60		µs
Settling Time to 0.5 LSB			10		µs
Offset Error	54, 55	–	–	±20	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity	54, 55	–	–	±4	LSBs
Differential Non-linearity	52, 54	–	–	±1	LSBs

Notes:

50 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

51 Typical – based on a 19.2MHz external oscillator

52 Guaranteed monotonic with no missing codes.

54 Specified between 2.5% and 97.5% of the full-scale range.

55 Calculated from the line of best fit of all the measured codes.

8.1.4 Parametric Performance

Details in this section represent provisional values.

For the following conditions unless otherwise specified:

External components as recommended in Section 5.
Maximum load on digital outputs = 30pF.
Clock source = 19.2MHz (clock input); T_{AMB} = +25°C.
AV_{DD} = DV_{DD} = 3.3V

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current					
Rx Mode					
DI_{DD} (Search for FS)		–	11.5	–	mA
DI_{DD} (FS found)		-	10	–	mA
AI_{DD}		-	7.5	–	mA
Tx Mode					
DI_{DD}		–	3.5	–	mA
AI_{DD}		–	8.5	–	mA
Idle Mode					
DI_{DD}		–	2	–	mA
AI_{DD}		–	0.6	–	mA

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modem Symbol Rate			4800		sym s^{-1}
Modulation			4-FSK		
Filter RRC Alpha			0.2		
Rx Co-channel Rejection	70	-	10.5	-	dB
Rx Adjacent Channel Rejection	70	-	66	-	dB
Tx Adjacent Channel Power	70,71	-	61	-	dB

Notes:

70 Test method based on ETSI EN 300 113-1
71 Modulation Deviation = 1944 Hz

8.2 C-BUS Timing

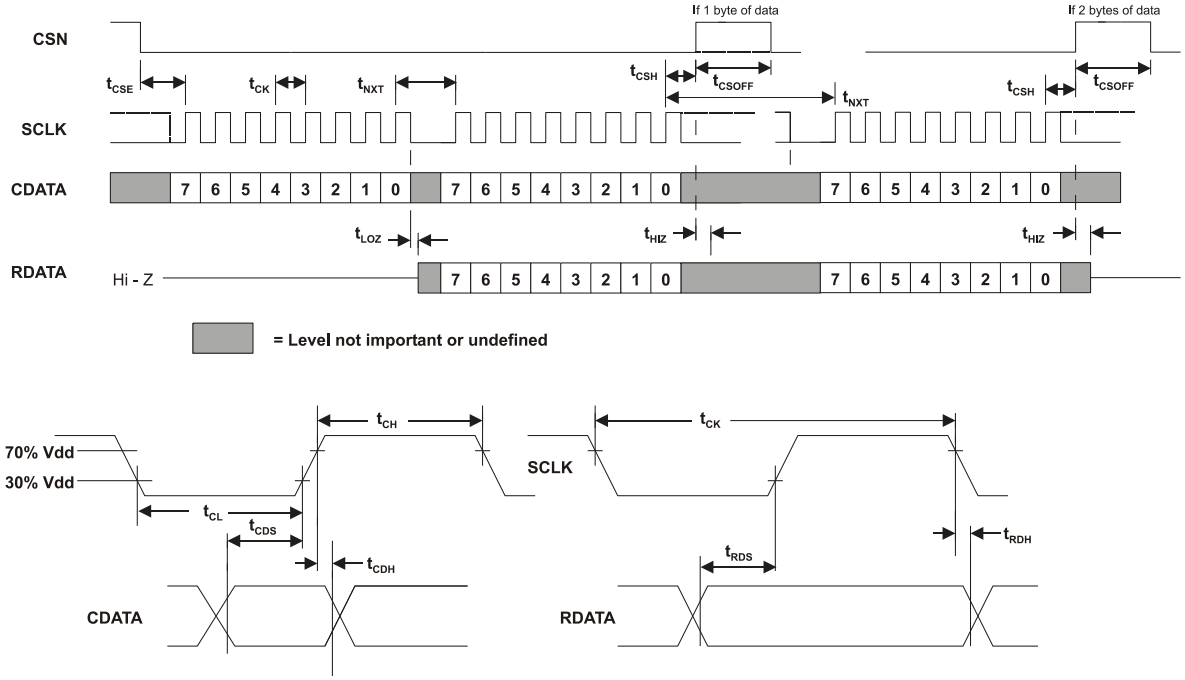


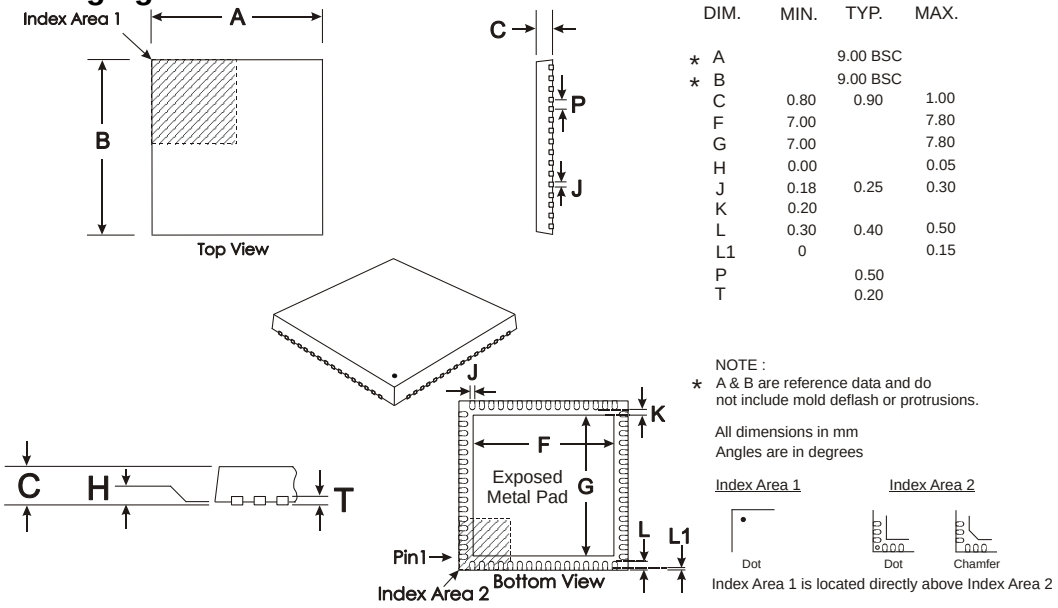
Figure 18 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA output enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		100	–	–	ns
t_{CK}	SCLK cycle time		100	–	–	ns
t_{CH}	SCLK high time		50	–	–	ns
t_{CL}	SCLK low time		50	–	–	ns
t_{CDS}	CDATA set-up time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA set-up time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon between the last rising edge of SCLK of each command and the rising edge of the CSN signal.
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7161 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

8.3 Packaging



DIM.	MIN.	TYP.	MAX.
* A		9.00 BSC	
* B		9.00 BSC	
C	0.80	0.90	1.00
F	7.00		7.80
G	7.00		7.80
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

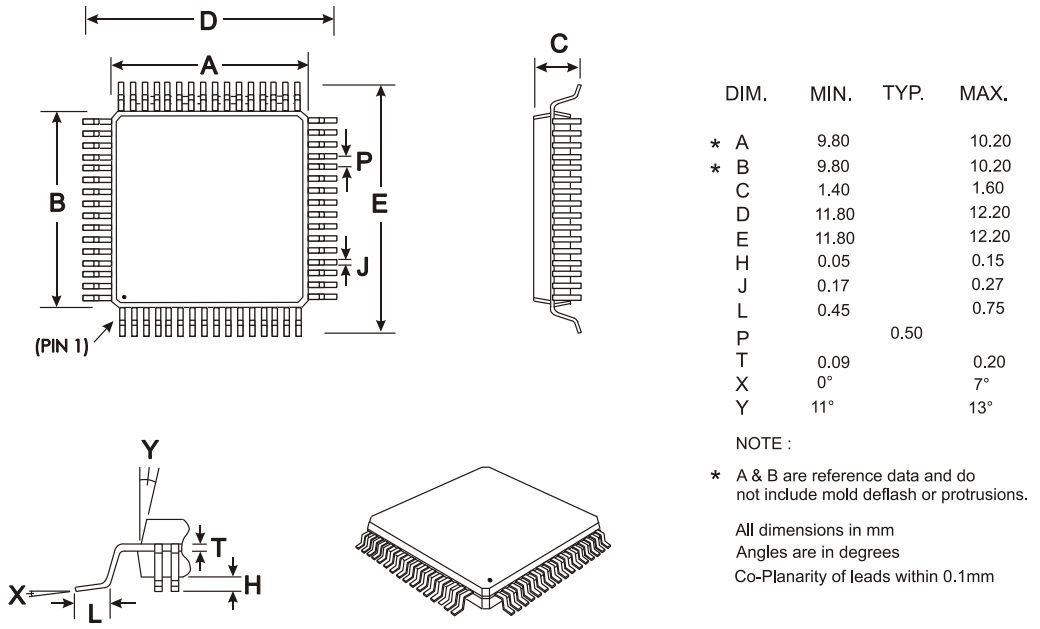
NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 19 Mechanical Outline of 64-lead VQFN (Q1)

Order as part no. CMX7161Q1



DIM.	MIN.	TYP.	MAX.
* A	9.80		10.20
* B	9.80		10.20
C	1.40		1.60
D	11.80		12.20
E	11.80		12.20
H	0.05		0.15
J	0.17		0.27
L	0.45		0.75
P		0.50	
T	0.09		0.20
X	0°		7°
Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 20 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7161L9

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support/Package Information page of the CML website: [www.cmlmicro.com].

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